The Claims:

The following is a listing of the claims:

1. (Previously Presented): A process for forming a contact opening to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of semiconductor material;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

selectively removing by said etch process at a total etch pressure in the range from about 1 millitorr to about 400 millitorr and by using an etchant selected from the group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, a portion of said doped silicon dioxide layer at a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

2. (Original): A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist; and

etching said doped silicon dioxide layer through the pattern of said layer of photoresist.

3. (Original): A process as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

4. (Original): A process as recited in Claim 1, wherein selective removing said doped silicon dioxide layer comprises a plasma etching process for etching said doped silicon dioxide layer in a plasma etcher.

5. (Previously Presented): A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3.

6. (Previously Presented):A process as recited in Claim 4, wherein said plasma etching process is conducted in a pressure range from about 1 millitorr to about 100 millitorr.

7. (Original): A process as recited in Claim 4, wherein during said plasma etching process said reactor cathode has a temperature range from about 10°C to about 80°C.

8. (Original): A process as recited in Claim 4, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

9. (Previously Presented): A process as defined in Claim 1, wherein said material removal rate is at least 10 times higher for doped silicon dioxide layer than for undoped silicon dioxide or for said layer of semiconductor material.

10. (Original): A process as defined in Claim 9, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of CH_2F_2 and CH_3F.

11. (Canceled).

12. (Original): A process as recited in Claim 1, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

13. (Previously Presented): A process for forming contact to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of monocrystalline silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

etching with said etch process said doped silicon dioxide layer through the pattern of said layer of photoresist at a material removal rate that is higher for doped silicon dioxide layer than for undoped silicon dioxide layer or for said layer of monocrystalline silicon to form an opening extending to said layer of monocrystalline silicon, said etching being a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 with a fluorinated chemical etchant selected from the

group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof.

14. (Original): A process as recited in Claim 13, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

15. (Canceled).

16. (Original): A process as defined in Claim 13, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group of CH_2F_2 and CH_3F.

17. (Original): A process as recited in Claim 13, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said semiconductor material.

18. (Previously Presented): A process for forming a contact to a semiconductor substrate comprising:

providing a gate oxide layer over the semiconductor substrate;

providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and an undoped silicon dioxide layer extending over said conductive layer;

forming a spacer, comprised of undoped silicon dioxide, adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

selectively removing with said etch process a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer, and the semiconductor substrate.

19. (Previously Presented): A process for forming a contact to a semiconductor substrate comprising:

providing a gate oxide layer over the semiconductor substrate;

providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and an undoped silicon dioxide layer extending over said conductive layer, wherein each said gate stack is formed by:

forming a polysilicon layer over said gate oxide layer;

forming a refractory metal silicide layer over said polysilicon layer; and

forming an undoped silicon dioxide layer over said refractory metal silicide layer;

forming a spacer, comprised of undoped silicon dioxide, adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

selectively removing with said etch process a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching

removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer, and the semiconductor substrate.

20. (Previously Presented): A process as recited in Claim 19, further comprising selectively removing portions of said undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer.

Claims 21-23 (Canceled).

24. (Original): A process as recited in Claim 18, wherein the semiconductor material is monocrystalline silicon.

25. (Original): A process as recited in Claim 18, wherein said plasma etcher is selected from the group consisting of an RF RIE etcher, a MERIE etcher, and a high density plasma etcher.

26. (Previously Presented): A process as recited in Claim 18, further comprising forming a contract plug comprising a conductive material and situated between said pair of gate stacks and over said surface on said semiconductor substrate.

27. (Previously Presented):A process as recited in Claim 20, wherein said refractory metal silicide layer is tungsten silicide.

28. (Original): A process as recited in Claim 18, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

29. (Previously Presented): A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist; and

etching with said etch process said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3; and

with a fluorinated chemical etchant.

30. (Previously Presented): A process as recited in Claim 29, wherein said fluorinated chemical etchants are selected from the group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof.

31. (Previously Presented): A process for forming a contact to a semiconductor material comprising:

depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

depositing a polysilicon layer over said gate oxide layer;

depositing a refractory metal silicide layer over said polysilicon layer;

depositing an undoped silicon dioxide layer over said refractory metal silicide layer;

selectively removing portions of said undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side perpendicular to said gate oxide layer and being comprised of:

said undoped silicon dioxide layer as the top layer thereof;

said refractory metal silicide layer;

said polysilicon layer; and

said gate oxide layer as the bottom layer thereof;

forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon

dioxide layer is selected from the group consisting of BPSG, PSG, and BSG; and

etching with said etch process said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 in an etcher selected from the group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof.

32. (Previously Presented): A process as recited in Claim 31, wherein the spacer material comprises one of silicon nitride and undoped silicon dioxide.

33. (Previously Presented): A process as recited in Claim 31, further comprising forming a contact plug comprising a conductive material and situated between said pair of gate stacks and over the exposed portion of said silicon layer.

34. (Previously Presented): A process as recited in Claim 31, wherein the material removal rate is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide.

35. (Original): A process as recited in Claim 31, wherein during etching of said doped silicon dioxide layer with said plasma etching system, the temperature range of said reactor cathode is from about 10°C to about 80°C.

36. (Original): A process as recited in Claim 31, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

37. (Previously Presented): A process for forming a gate structure comprising:

providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

removing said first layer of photoresist;

depositing a doped silicon dioxide layer over said multilayer structure;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

etching with said etch process said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch that is an anisotropic plasma etch using fluorinated chemical etchants selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, and that etches through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material;

removing said second layer of photoresist; and

forming a contact plug comprised of a conductive material in contact with said contact surface on said layer of silicon.

38. (Original): A process as recited in Claim 37, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

39. (Canceled).

40. (Original): A process as recited in Claim 37, wherein said multilayer structure further comprises layers of gate oxide, polysilicon, and refractory metal silicide.

41. (Previously Presented): A process as recited in Claim 37, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

42. (Previously Presented): A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch utilizes a plasma etching system selected from the group consisting of RF RIE, MERIE system, and a high density plasma etch system.

43. (Previously Presented): A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch is a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3; and

with a fluorinated chemical etchant.

44. (Previously Presented): A process for forming a gate structure comprising:

providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

removing said first layer of photoresist;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped

silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG;

forming a second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

etching with said etch process said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, wherein said etching of said doped silicon dioxide utilizes a plasma etching system having a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3 at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

removing said second layer of photoresist; and

forming a contact plug comprising a conductive material in contact with said contact surface on said layer of silicon.

45. (Canceled).

46. (Original): A process as recited in Claim 44, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

Claims 47-49 (Canceled).

50. (Previously Presented): A method of forming a self-aligned contact, said method comprising:

providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by an undoped silicon dioxide layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

forming a layer of photoresist over said silicon dioxide layer;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

patterning said layer of photoresist; and

selectively removing with said etch process a portion of said doped silicon dioxide layer between said pair of gate stacks using an etchant selected from the group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing less of said updoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

51. (Previously Presented): A method as recited in Claim 50, wherein said selective removal of said doped silicon dioxide layer comprises a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C; and

in a plasma density in a range from about 10^9 ions/cm^3 to about 10^{13} ions/cm^3.

52. (Original): A method as recited in Claim 51, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

53. (Canceled).

54. (Previously Presented): A method as recited in Claim 51, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for semiconductor material.

55. (Previously Presented): A process as recited in Claim 1, wherein said doped silicon dioxide layer consists of BSG.

56. (Previously Presented): A process as recited in Claim 18, wherein said doped silicon dioxide layer consists of BSG.

57. (Previously Presented): A process as recited in Claim 37, wherein said doped silicon dioxide layer consists of BSG.

58. (Previously Presented): A process for forming a contact opening to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of semiconductor material;

selecting an etch process that is selective to undoped silicon dioxide and to silicon;

forming a BSG layer over said undoped silicon dioxide layer; and

selectively removing by said etch process at a total etch pressure in the range from about 1 millitorr to about 400 millitorr and by using an etchant selected from the group consisting of C_2F_6, C_3F_8, C_4F_{10}, CH_2F_2, C_2HF_5, CH_3F, and combinations thereof, a portion of said doped silicon dioxide layer at a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

59. (Previously Presented): The process of claim 1 wherein the etchant comprises C_2F_6.

60. (Previously Presented): The process of claim 1 wherein the etchant comprises C_3F_8.

61. (Previously Presented): The process of claim 1 wherein the etchant comprises C_4F_{10}.

62. (Previously Presented): The process of claim 1 wherein the etchant comprises CH_2F_2.

63. (Previously Presented): The process of claim 1 wherein the etchant comprises C_2HF_5.

64. (Previously Presented): The process of claim 1 wherein the etchant comprises CH_3F.

65. (Previously Presented): The process of claim 13 wherein the etchant comprises C_2F_6.

66. (Previously Presented): The process of claim 13 wherein the etchant comprises C_3F_8.

67. (Previously Presented): The process of claim 13 wherein the etchant comprises C_4F_{10}.

68. (Previously Presented): The process of claim 13 wherein the etchant comprises CH_2F_2.

69. (Previously Presented): The process of claim 13 wherein the etchant comprises C_2HF_5.

70. (Previously Presented): The process of claim 13 wherein the etchant comprises CH_3F.

71. (Previously Presented): The process of claim 31 wherein the etchant comprises C_2F_6.

72. (Previously Presented): The process of claim 31 wherein the etchant comprises C_3F_8.

73. (Previously Presented): The process of claim 31 wherein the etchant comprises C_4F_{10}.

74. (Previously Presented): The process of claim 31 wherein the etchant comprises CH_2F_2.

75. (Previously Presented): The process of claim 31 wherein the etchant comprises C_2HF_5.

76. (Previously Presented): The process of claim 31 wherein the etchant comprises CH_3F.

77. (Previously Presented): The process of claim 37 wherein the etchant comprises C_2F_6.

78. (Previously Presented): The process of claim 37 wherein the etchant comprises C_3F_8.

79. (Previously Presented): The process of claim 37 wherein the etchant comprises C_4F_{10}.

80. (Previously Presented): The process of claim 37 wherein the etchant comprises CH_2F_2.

81. (Previously Presented): The process of claim 37 wherein the etchant comprises C_2HF_5.

82. (Previously Presented): The process of claim 37 wherein the etchant comprises CH_3F.

83. (Previously Presented): The process of claim 44 wherein the etchant comprises C_2F_6.

84. (Previously Presented): The process of claim 44 wherein the etchant comprises C_3F_8.

85. (Previously Presented): The process of claim 44 wherein the etchant comprises C_4F_{10}.

86. (Previously Presented): The process of claim 44 wherein the etchant comprises CH_2F_2.

87. (Previously Presented): The process of claim 44 wherein the etchant comprises C_2HF_5.

88. (Previously Presented): The process of claim 44 wherein the etchant comprises CH_3F.

89. (Previously Presented): The process of claim 50 wherein the etchant comprises C_2F_6.

90. (Previously Presented): The process of claim 50 wherein the etchant comprises C_3F_8.

91. (Previously Presented): The process of claim 50 wherein the etchant comprises C_4F_{10}.

92. (Previously Presented): The process of claim 50 wherein the etchant comprises CH_2F_2.

93. (Previously Presented): The process of claim 50 wherein the etchant comprises C_2HF_5.

94. (Previously Presented): The process of claim 50 wherein the etchant comprises CH_3F.

95. (Previously Presented): The process of claim 58 wherein the etchant comprises C_2F_6.

96. (Previously Presented): The process of claim 58 wherein the etchant comprises C_3F_8.

97. (Previously Presented): The process of claim 58 wherein the etchant comprises C_4F_{10}.

98. (Previously Presented): The process of claim 58 wherein the etchant comprises CH_2F_2.

99. (Previously Presented): The process of claim 58 wherein the etchant comprises C_2HF_5.

100. (Previously Presented): The process of claim 58 wherein the etchant comprises CH_3F.

101. (Previously Presented): The method of claim 1 wherein said selecting an etch process is also selective to silicon nitride.

102. (Previously Presented): The method of claim 13 wherein said selecting an etch process is also selective to silicon nitride.

103. (Previously Presented): The method of claim 18 wherein said selecting an etch process is also selective to silicon nitride.

104. (Previously Presented): The method of claim 19 wherein said selecting an etch process is also selective to silicon nitride.

105. (Previously Presented): The method of claim 31 wherein said selecting an etch process is also selective to silicon nitride.

106. (Previously Presented): The method of claim 37 wherein said selecting an etch process is also selective to silicon nitride.

107. (Previously Presented): The method of claim 44 wherein said selecting an etch process is also selective to silicon nitride.

108. (Previously Presented): The method of claim 50 wherein said selecting an etch process is also selective to silicon nitride.

109. (Previously Presented): The method of claim 58 wherein said selecting an etch process is also selective to silicon nitride.